Fig.1

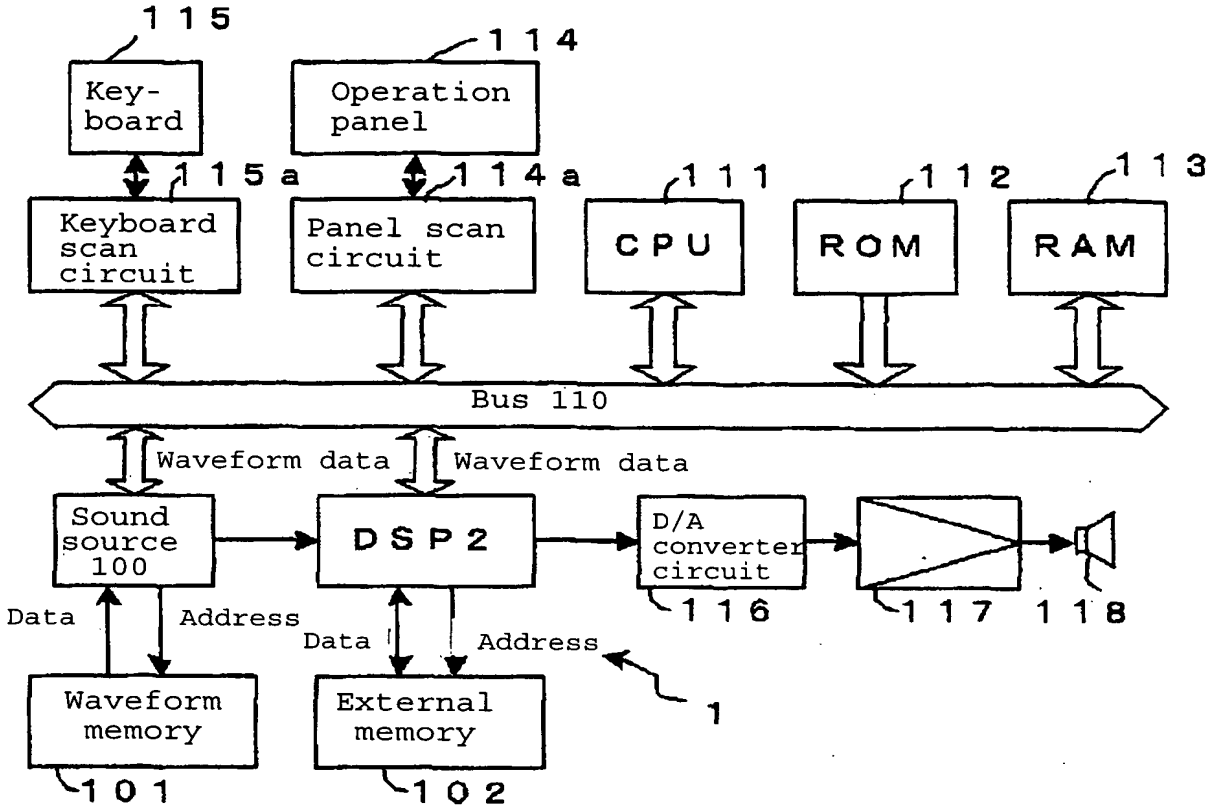

115
Key-board
114
Operation panel
115a
114a
111
112
113
Keyboard scan circuit
Panel scan circuit
CPU
ROM
RAM
Bus 110
Waveform data
Waveform data
Sound source 100
DSP2
D/A converter circuit
116
117
118
Data
Address
Data
Address
1
Waveform memory
External memory
101
102

Fig.2

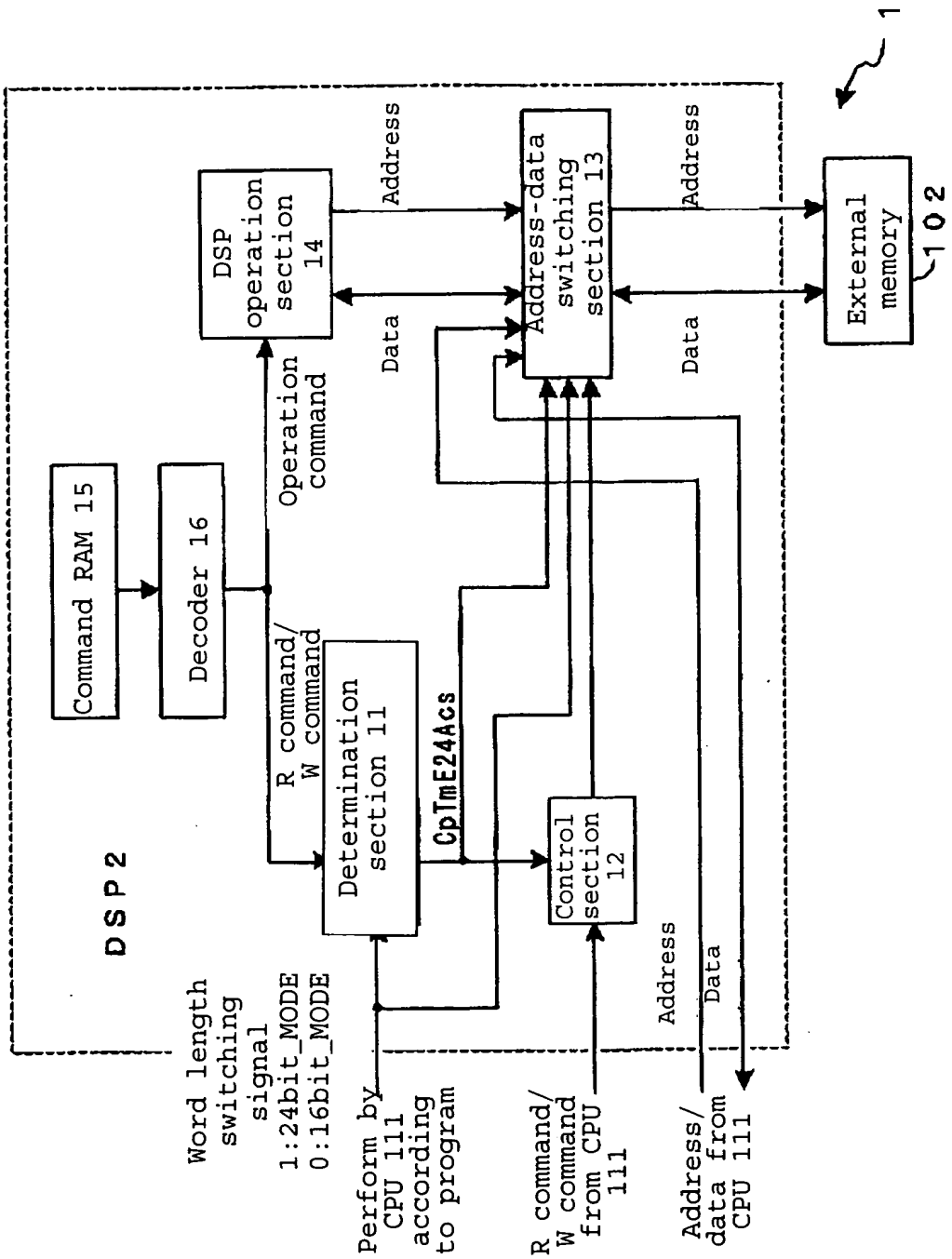

1
DSP 2
Command RAM 15
Decoder 16
Operation command
DSP operation section 14
Address
Data
Address-data switching section 13
Address
Data
External memory
102
R command/ W command
Determination section 11
CpTmE24Acs
Control section 12
Word length switching signal 1:24bit_MODE 0:16bit_MODE
Perform by CPU 111 according to program
R command/ W command from CPU 111
Address/ data from CPU 111
Address
Data

Fig.3

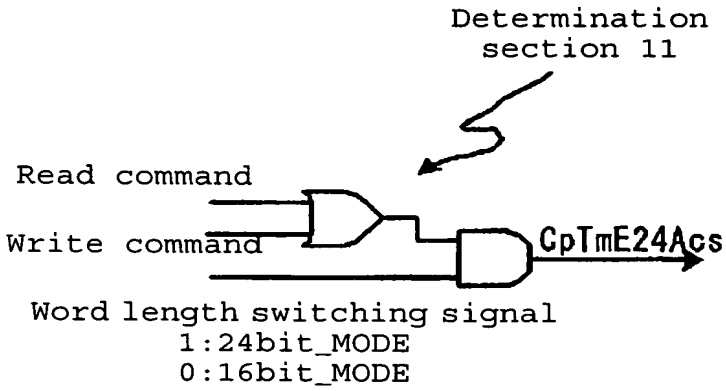


Fig.4

		CpTmE24Acs
24bit_MODE (1)	R	1
	W	1
	N	0
16bit_MODE (0)	R	0
	W	0
	N	0

CpTmE24Acs=0
When CPU 111 is allowed to access

Fig.5

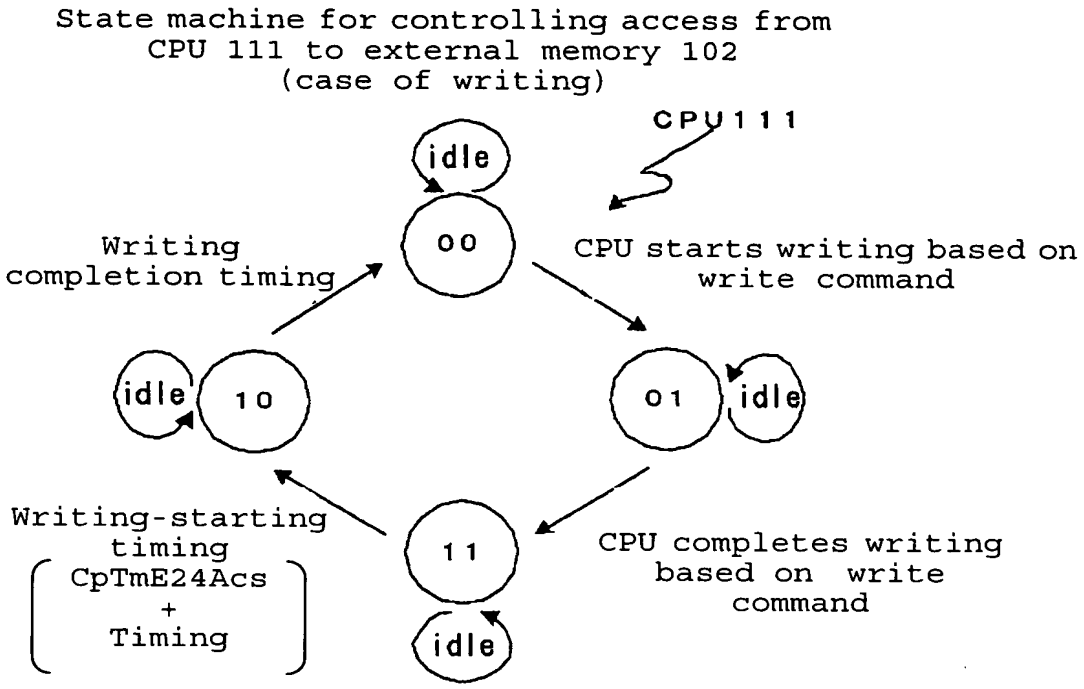
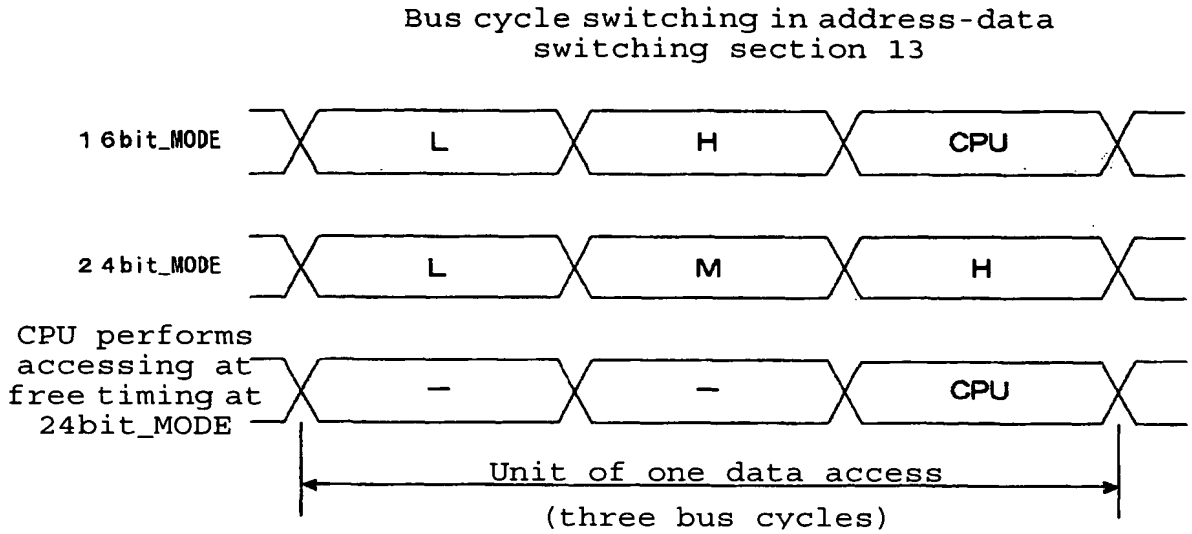

State machine for controlling access from CPU 111 to external memory 102 (case of writing)
CPU111
idle
00
Writing completion timing
CPU starts writing based on write command
idle
10
01
idle
Writing-starting timing
CpTmE24Acs
+
Timing
11
CPU completes writing based on write command
idle

Fig.6



16bit_MODE
L: access to low-order byte of 16 bits
H: access to high-order byte of 16 bits
CPU: access from CPU

24bit_MODE
L: access to low-order byte of 24 bits
M: access to middle-order byte of 24 bits
H: access to high-order byte of 24 bits
CPU: access from CPU
-: no access

Fig.7

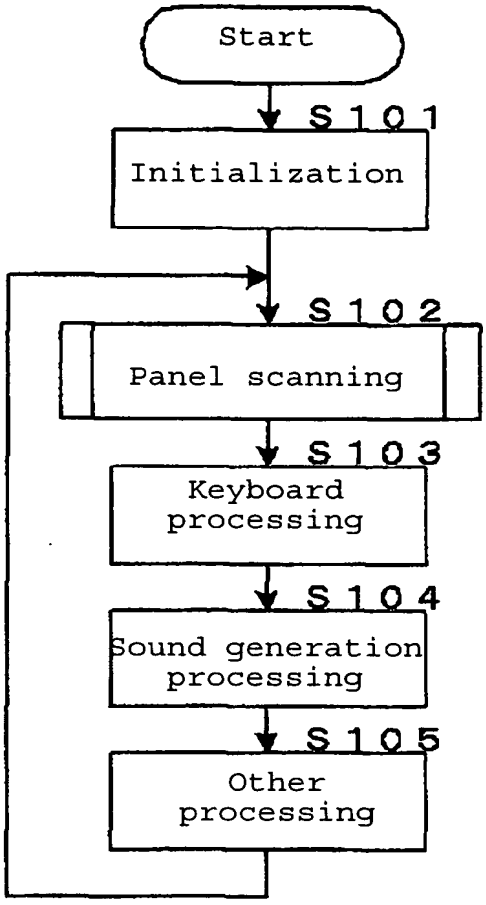

Start
S101
Initialization
S102
Panel scanning
S103
Keyboard processing
S104
Sound generation processing
S105
Other processing

Fig.8

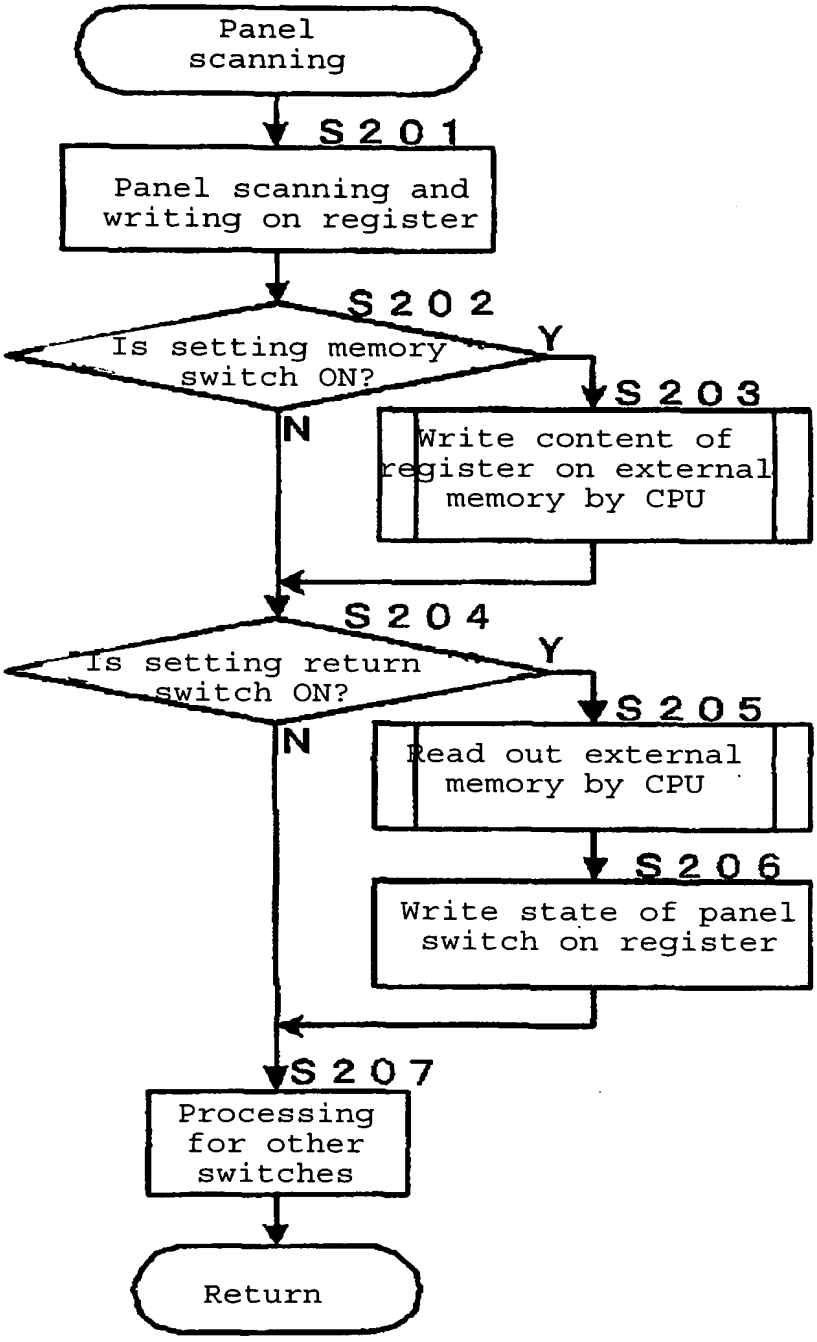

Panel scanning
S201
Panel scanning and writing on register
S202
Is setting memory switch ON?
Y
N
S203
Write content of register on external memory by CPU
S204
Is setting return switch ON?
Y
N
S205
Read out external memory by CPU
S206
Write state of panel switch on register
S207
Processing for other switches
Return

Fig.9

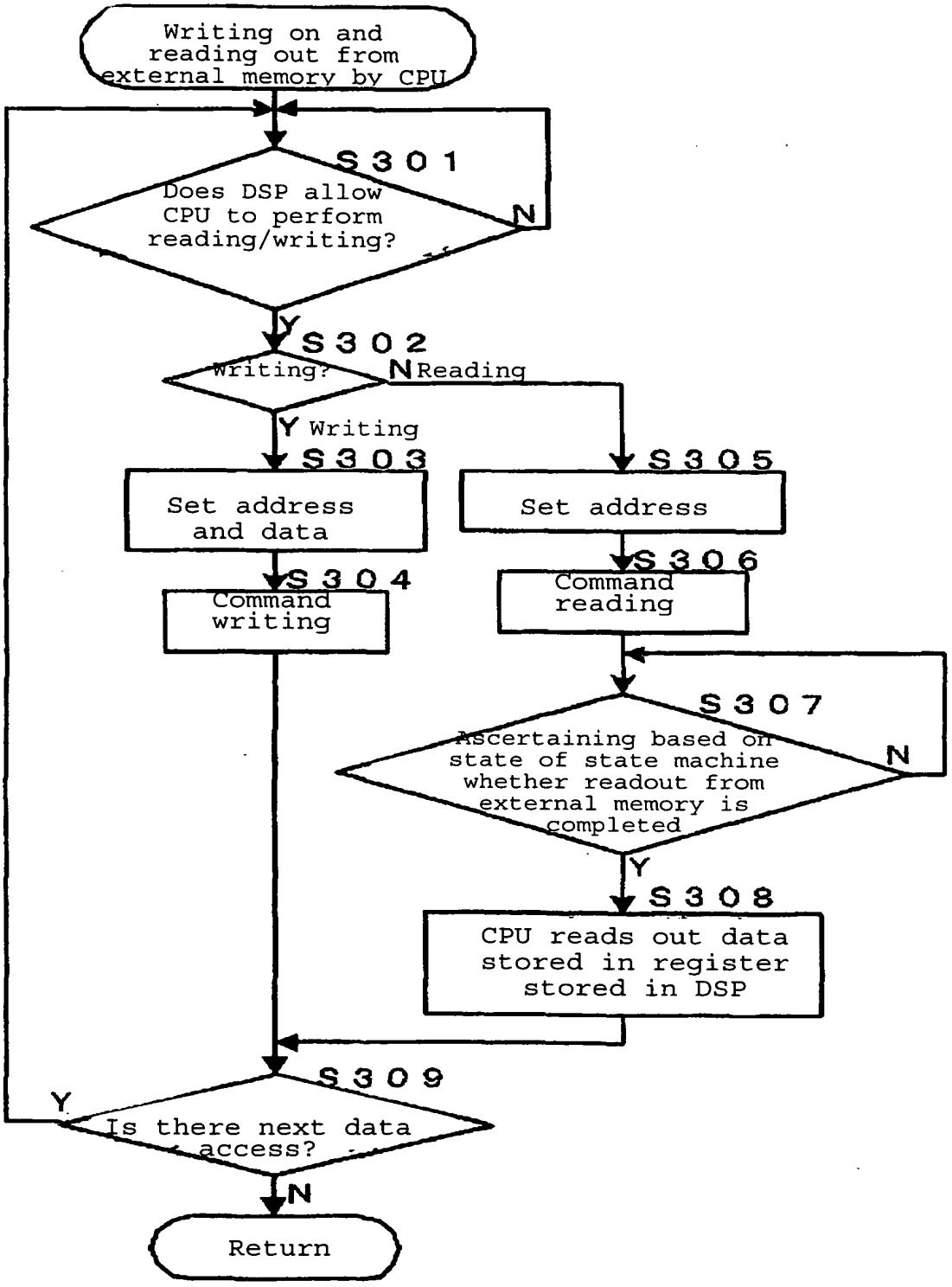

Writing on and reading out from external memory by CPU
S301
Does DSP allow CPU to perform reading/writing?
N
Y
S302
Writing?
N Reading
Y Writing
S303
Set address and data
S304
Command writing
S305
Set address
S306
Command reading
S307
Ascertaining based on state of state machine whether readout from external memory is completed
N
Y
S308
CPU reads out data stored in register stored in DSP
S309
Y
Is there next data access?
N
Return

Fig.10

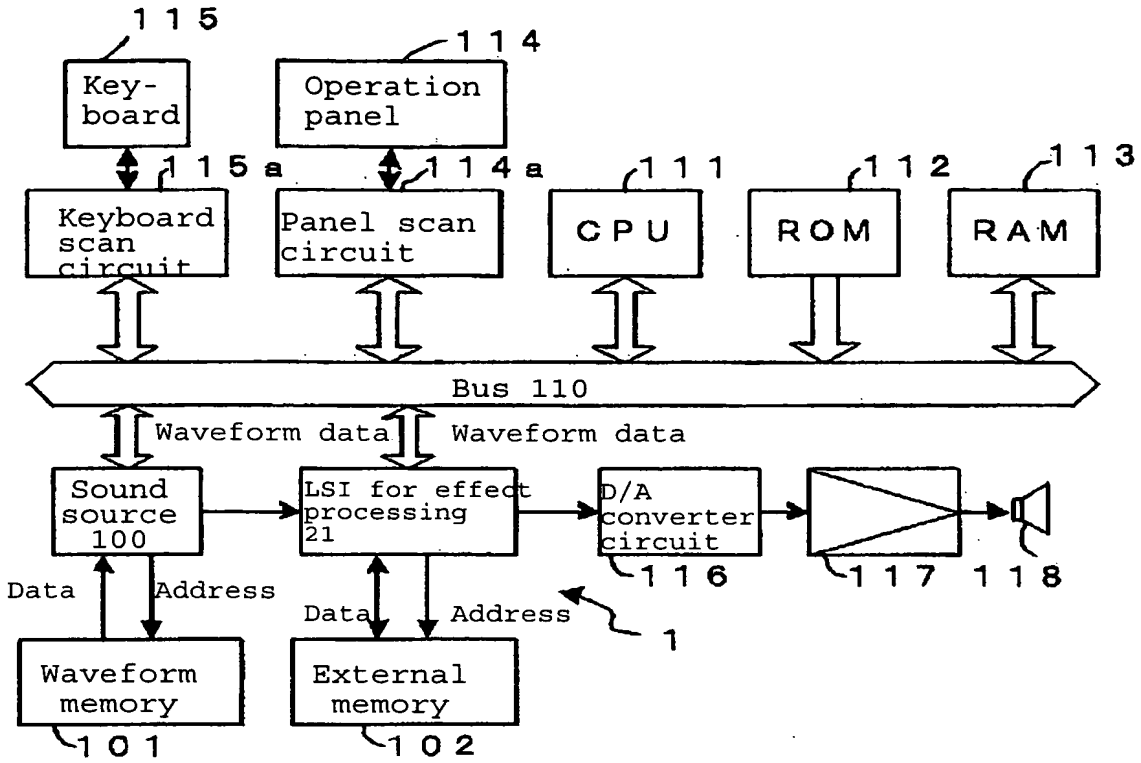

115
Key-board
114
Operation panel
115a
114a
111
112
113
Keyboard scan circuit
Panel scan circuit
CPU
ROM
RAM
Bus 110
Waveform data
Waveform data
Sound source 100
LSI for effect processing 21
D/A converter circuit
116
117
118
Data
Address
Data
Address
1
Waveform memory
101
External memory
102

Fig.11

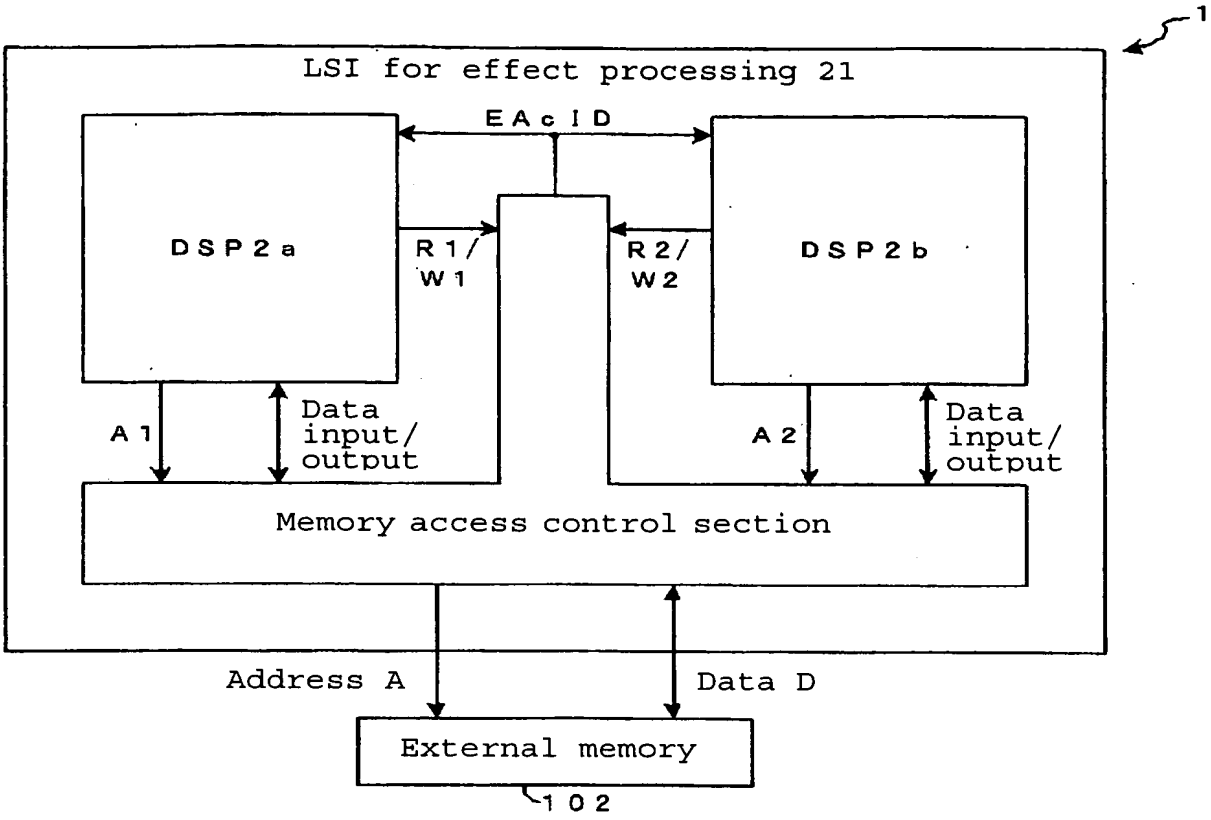

1
LSI for effect processing 21
EAcID
DSP2a
DSP2b
R1/
W1
R2/
W2
A1
Data
input/
output
A2
Data
input/
output
Memory access control section
Address A
Data D
External memory
102

Fig.12

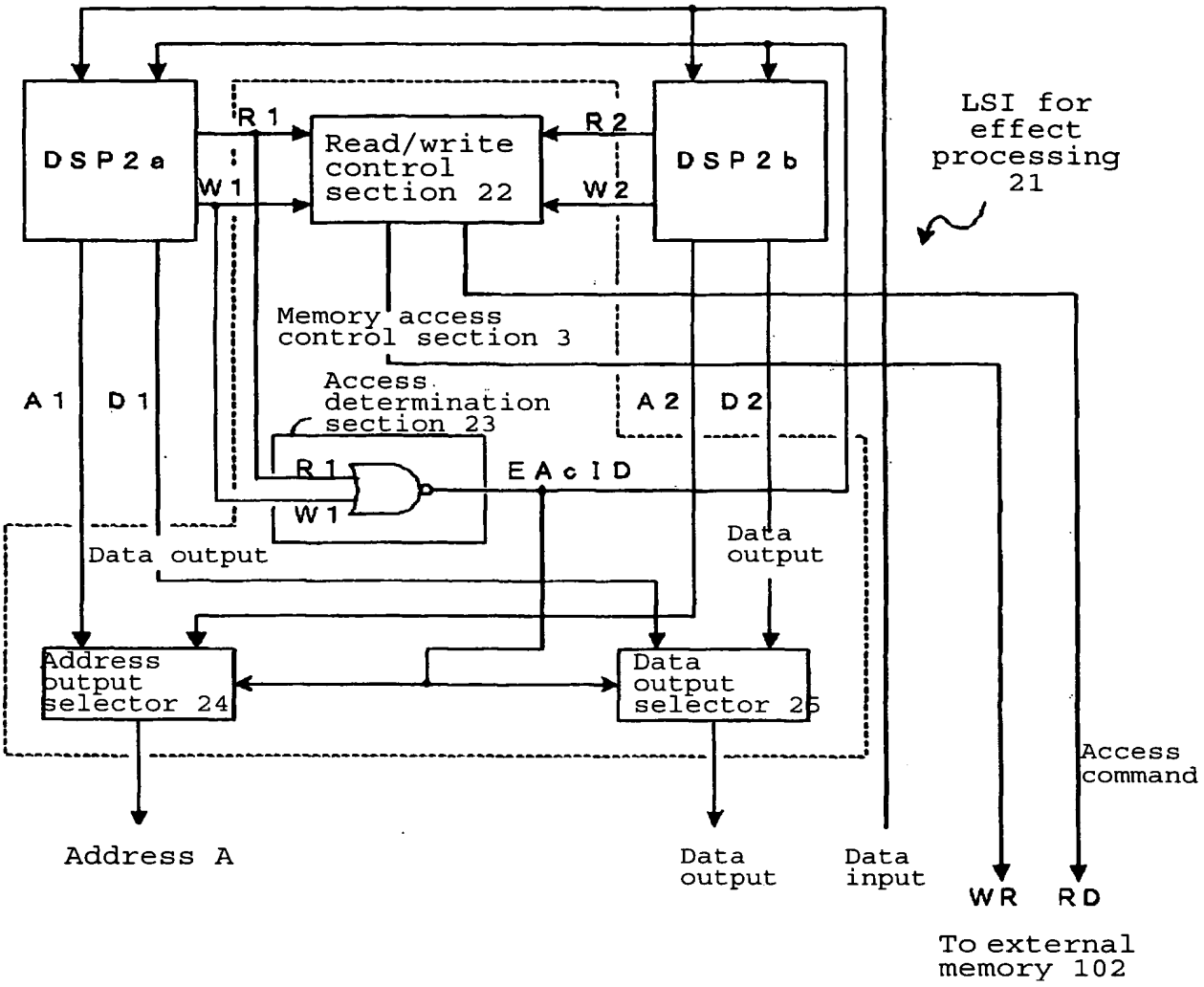

DSP2a
DSP2b
R1
W1
R2
W2
Read/write control section 22
LSI for effect processing 21
Memory access control section 3
A1
D1
A2
D2
Access determination section 23
R1
W1
EAcID
Data output
Data output
Address output selector 24
Data output selector 25
Access command
Address A
Data output
Data input
WR
RD
To external memory 102

Fig.13

DSP2a	DSP2b	After control
R1	R2	N
R1	W2	N
R1	N	R1
W1	R2	N
W1	W2	N
W1	N	W1
N	R2	R2
N	W2	W2
N	N	N

R: read
W: write
N: no access

Fig.14

R1	W1	EAcID	
0	0	1	DSP2b
1	0	0	DSP2a
0	1	0	DSP2a

Fig.15

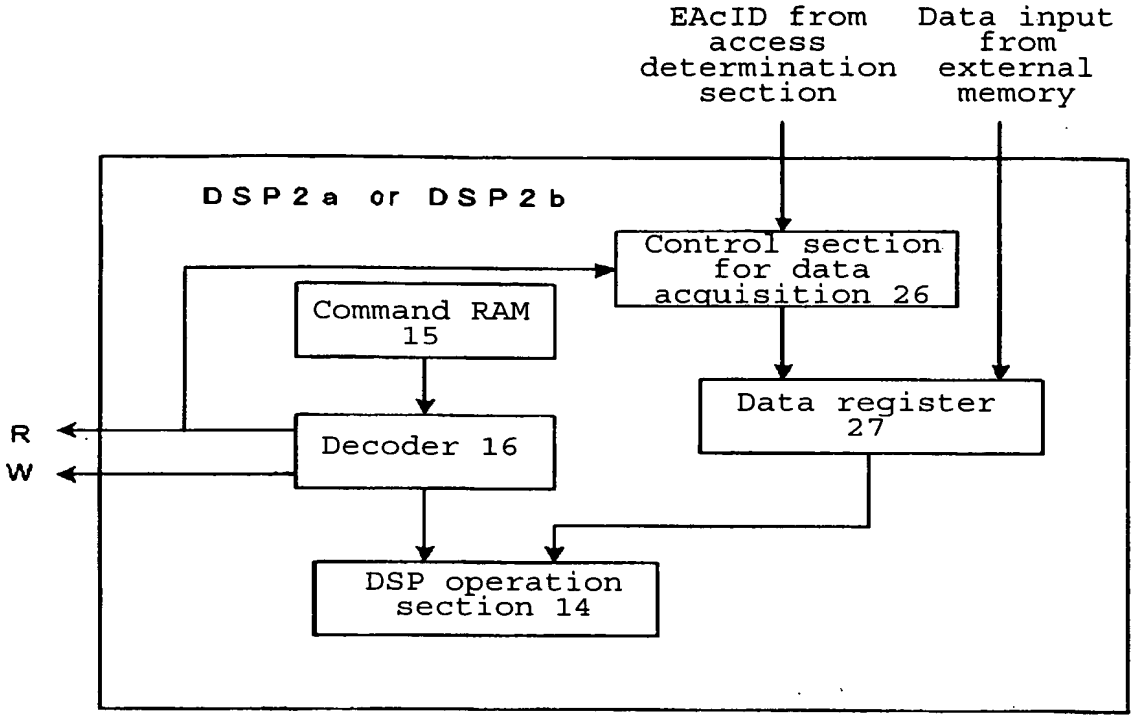

EAcID from access determination section
Data input from external memory
DSP2a or DSP2b
Control section for data acquisition 26
Command RAM 15
Data register 27
R
W
Decoder 16
DSP operation section 14

Fig.16

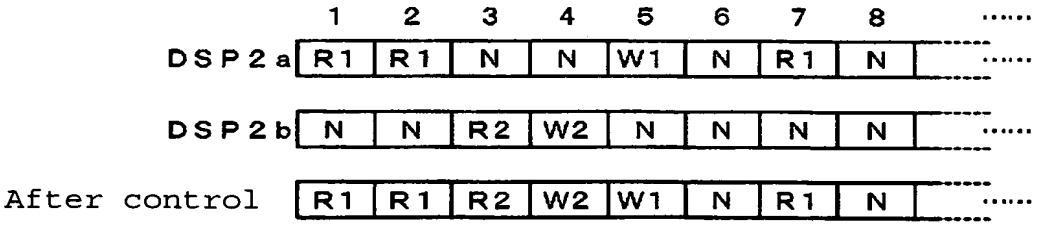

1 2 3 4 5 6 7 8
DSP2a R1 R1 N N W1 N R1 N
DSP2b N N R2 W2 N N N N
After control R1 R1 R2 W2 W1 N R1 N

Fig.17

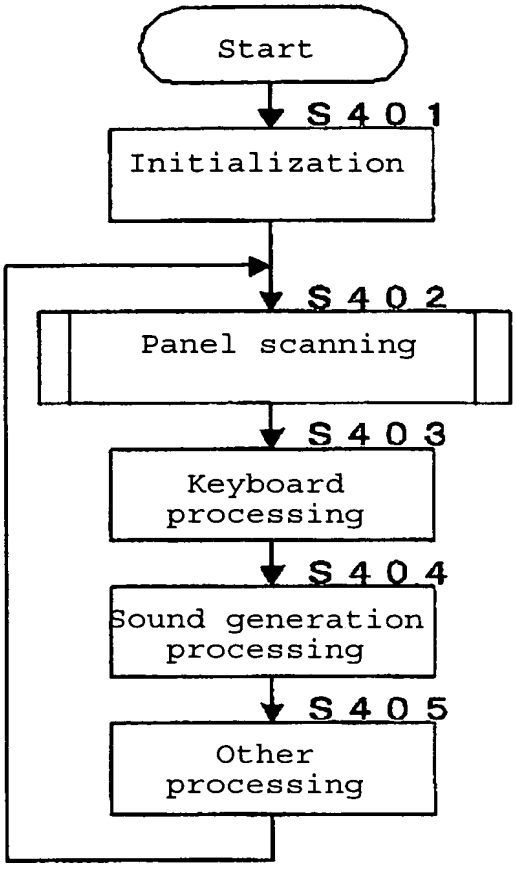

Start
S401
Initialization
S402
Panel scanning
S403
Keyboard processing
S404
Sound generation processing
S405
Other processing

Fig.18

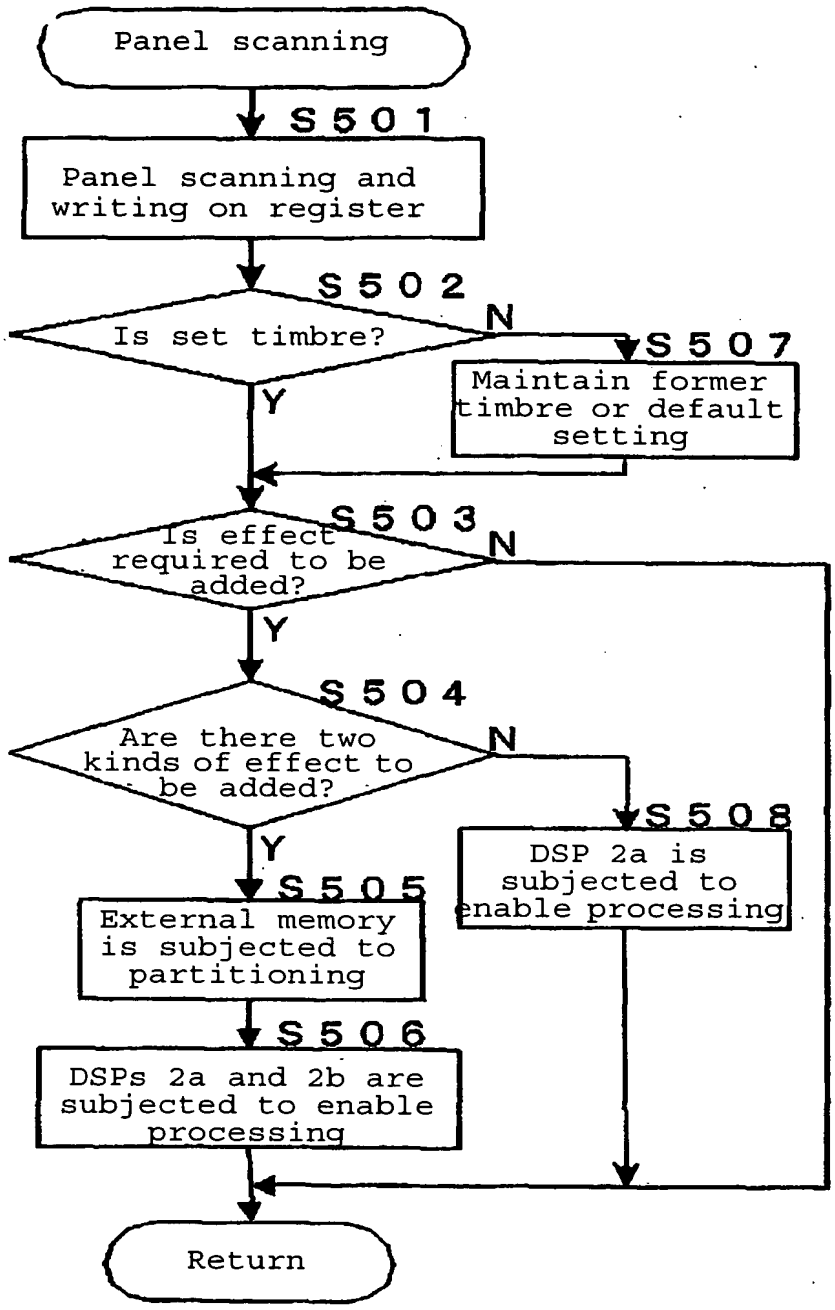

Panel scanning
S501
Panel scanning and writing on register
S502
Is set timbre?
N
S507
Maintain former timbre or default setting
Y
S503
Is effect required to be added?
N
Y
S504
Are there two kinds of effect to be added?
N
S508
DSP 2a is subjected to enable processing
Y
S505
External memory is subjected to partitioning
S506
DSPs 2a and 2b are subjected to enable processing
Return

Fig.19

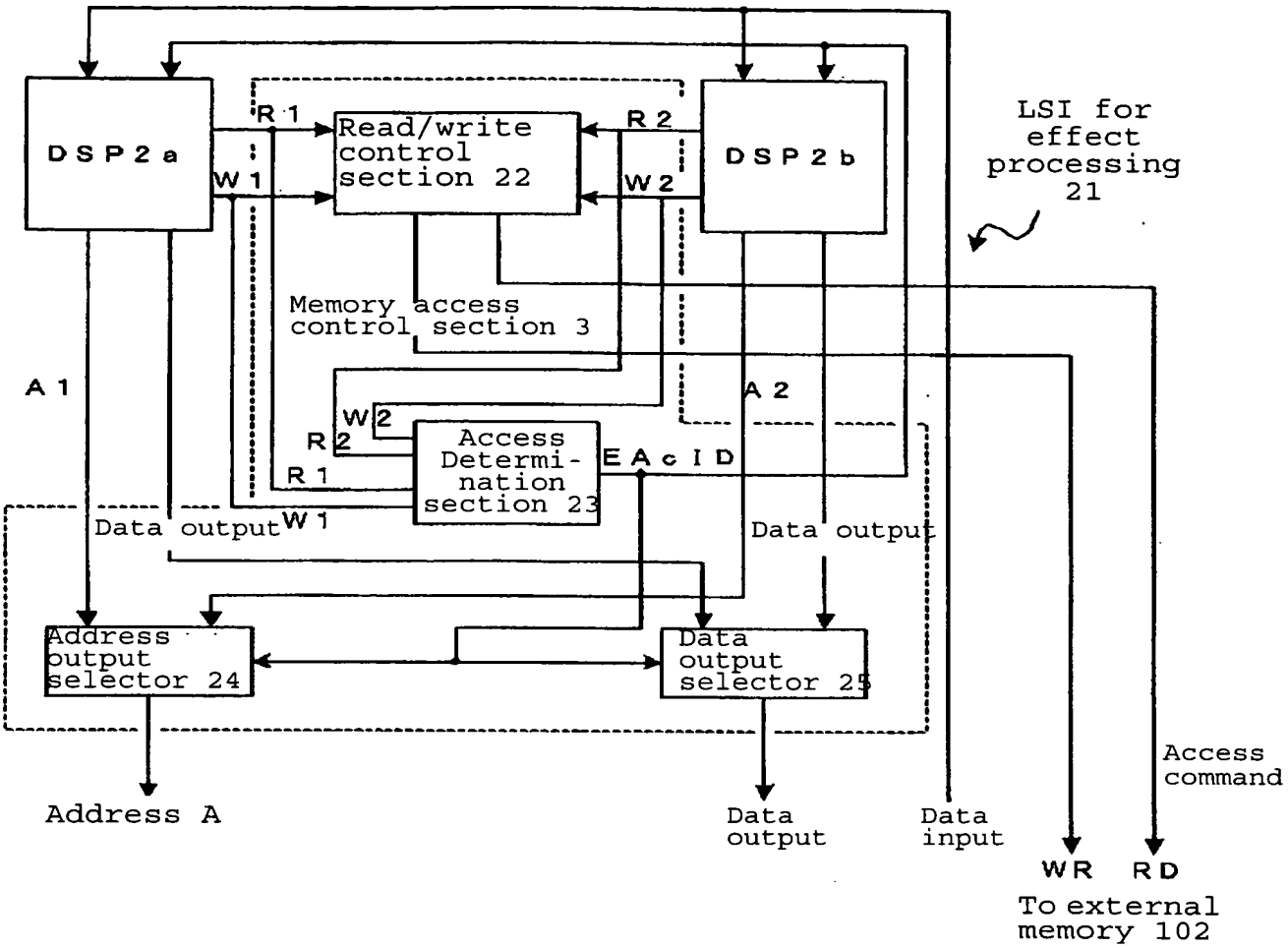
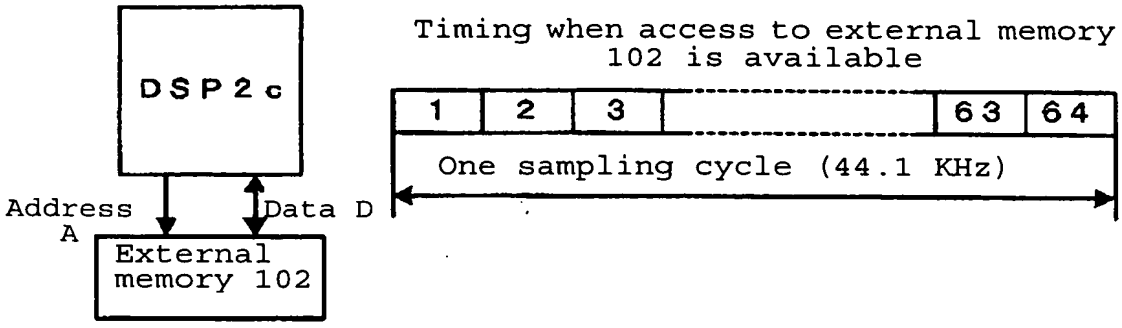

DSP2a
DSP2b
R1
W1
R2
W2
Read/write control section 22
LSI for effect processing 21
Memory access control section 3
A1
A2
W2
R2
R1
W1
Access Determination section 23
EAcID
Data output
Data output
Address output selector 24
Data output selector 25
Address A
Data output
Data input
Access command
WR
RD
To external memory 102

Fig.20


DSP2c
Address A
Data D
External memory 102
Timing when access to external memory 102 is available
1
2
3
63
64
One sampling cycle (44.1 KHz)